TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No. OKI.618

In Re Application Of: **Shunji Takase**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/761,224	January 22, 2004	F. Erdem	20987	2826	2746

Invention: **SEMICONDUCTOR DEVICE**

COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **November 14, 2005.**

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Dated: **January 11, 2006**

ANDREW J. TELESZ, JR.
REG. NO. 33,581

VOLENTINE FRANCOS & WHITT, P.L.L.C.
11951 FREEDOM DRIVE, SUITE 1260
RESTON, VA 20190
TEL. NO. (571) 283-0720

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	:	Before the Board of Appeals
Shunji Takase	:	Appeal No.:
Serial No.: 10/761,224	:	Group No.: 2826
Filed: January 22, 2004	:	Examiner: F. Erdem

For: SEMICONDUCTOR DEVICE

January 11, 2006

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In re Patent application of	:	
Shunji Takase	:	Group Art Unit: 2826
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APPEAL BRIEF

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Randolph Building
401 Dulany Street
Alexandria, VA 22314

Date: January 11, 2006

Sir:

In response to the Final Office Action dated August 11, 2005, and further responsive to the Notice of Appeal filed November 14, 2005, this corresponding Appeal Brief is respectfully submitted.

I. REAL PARTY IN INTEREST

This application is assigned to Oki Electric Industry Co., Ltd., which is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that may be related to, that will directly affect or be directly affected by or have a bearing on the Board's

Decision in this pending Appeal.

III. STATUS OF CLAIMS

The status of the claims as noted in the Advisory Action dated November 4, 2005, is as follows:

Claims 1-3, 5-7, 9-11 and 13-20 (rejected).

Claims 4, 8 and 12 (objected to).

Claims 1-3, 5-7, 9-11 and 13-20 have been finally rejected.

Accordingly, the rejection of claims 1-3, 5-7, 9-11 and 13-20 is being appealed.

IV. STATUS OF AMENDMENTS

Subsequent to the Final Office Action dated August 11, 2005, Appellant submitted a Request for Reconsideration dated October 11, 2005, without amending the pending claims. Thus, the claims have not been amended subsequent to the final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a semiconductor device equipped with fuses having reduced cross-sectional area, so that cross-section of wiring connected to the fuses may be reduced.

Accordingly, the invention, as broadly featured in independent claim 1, includes in combination a substrate (12 in Fig. 1); a first insulator layer (14)

formed on the substrate (12); a first conductive layer (16) formed on the first insulator layer (14); a second insulator layer (18) formed on the first conductive layer (16); the second insulator layer (18) including a through hole (24) having a substantially vertical side face (e.g., page 6, line 26 to page 7, line 4 and as shown in Fig. 1); a second conductive layer (20) formed on the second insulator layer (18) (e.g., page 6, lines 5-14 and as shown in Fig. 1); a dielectric sidewall structure (26) formed on the side face of the through hole (24) so that the dielectric sidewall structure (26) gradually narrows the through hole (24) (e.g., page 7, lines 5-10 and page 9, lines 3-11 and as shown in Fig. 1); and a fuse (32) formed on a conductive material that buries the narrowed through hole (24), said fuse (32) having a lower end connected to the first conductive layer (16) and an upper end connected to the second conductive layer (20) (e.g., page 7, lines 11-14 and as shown in Fig. 1).

As broadly featured in claim 3 as dependent upon claim 1, the dielectric sidewall structure (26) includes a first layer (28) formed on the side face of the through hole (24) and a second layer (30) formed on the first layer (28) (e.g., page 7, lines 5-8 and as shown in Fig. 1).

The invention, as broadly featured in independent claim 9, includes in combination a semiconductor substrate (12 as shown in Fig. 1); a first dielectric film (14) formed on the semiconductor substrate (12); a first conductive film (16) formed on the first dielectric film (14); a second dielectric film (18) formed on the first conductive film (16), the second dielectric film (18) including a through hole (24) (e.g., page 6, line 26 to page 7, line 4 and as

shown in Fig. 1) that exposes the first conductive film (16) (e.g., page 6, lines 5-14 and as shown in Fig. 1); a dielectric sidewall structure (26) formed on a side surface of the through hole (24) so that the dielectric sidewall structure (26) gradually narrows the through hole (24) (e.g., page 7, lines 5-10 and page 9, lines 3-11 and as shown in Fig. 1); a conductive material (32) filled in the narrowed through hole (24) (e.g., page 7, lines 11-14 and as shown in Fig. 1); and a second conductive film (20) on the second dielectric film (18) and the conductive material (16), so that the conductive material (32) electrically connects the first and second conductive films (16 and 20) to each other (e.g., page 6, lines 5-14 and as shown in Fig. 1).

As broadly featured in claim 11 as dependent upon claim 9, the dielectric sidewall structure (26) includes a first sidewall film (28) formed on the side surface of the through hole (24) and a second sidewall film (30) formed on the first sidewall film (28) (e.g., page 7, lines 5-8 and as shown in Fig. 1).

As broadly featured in claim 15 as dependent upon claim 11, the first sidewall film (28) is formed of silicon nitride and the second sidewall film (30) is formed of silicon oxide (e.g., page 7, lines 5-10 and as shown in Fig. 1).

The invention, as broadly featured in independent claim 16, includes in combination a semiconductor substrate (12 in Fig. 1); a first conductive film (16) formed on the semiconductor substrate (12); a dielectric film (18) formed on the first conductive film (16) and the semiconductor substrate (12), the dielectric film (16) having a through hole (24) (e.g., page 6, line 26 to page 7,

line 4 and as shown in Fig. 1) that exposes the first conductive film (16) (e.g., page 6, lines 5-14 and as shown in Fig. 1); a dielectric sidewall structure (26) formed in the through hole (24) so that the through hole (24) is gradually narrowed by the dielectric sidewall structure (26) to expose the first conductive film (16) (e.g., page 7, lines 5-10 and page 9, lines 3-11 and as shown in Fig. 1); a fuse structure formed by conductive material (32) filled in the narrow through hole (24) (e.g., page 7, lines 11-14 and as shown in Fig. 1); and a second conductive film (20) on the dielectric film (18) and the fuse structure (32), so that the fuse structure electrically connects the first and second conductive films (16 and 20) to each other (e.g., page 7, lines 11-14 and as shown in Fig. 1).

As broadly featured in claim 18 as dependent upon claim 16, the dielectric sidewall structure (26) includes a first sidewall film (28) formed on a side surface of the through hole (24) and a second sidewall film (30) formed on the first sidewall film (28) (e.g., page 7, lines 5-8 and as shown in Fig. 1).

VI. Grounds of Rejection to be Reviewed on Appeal

The issues on Appeal are:

(1) The rejection of claims 1-3, 5-7, 9-11 and 13-20 under 35 U.S.C. 103(a) as being unpatentable over the Weber et al. reference (U.S. Patent No. 6,242,789) in view of Japanese Patent Publication No. 4-348517) further in view of the Houston reference (U.S. Patent Application Publication No. 2002/0086465).

VII. Arguments

1) Claims 1-3, 5-7, 9-11 and 13-20 are patentable over the Weber et al. reference as taken with Japanese Patent Publication No. 4-348517 and the Houston reference

Claims 1-3, 5-7, 9-11 and 13-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Weber et al. reference in view of Japanese Patent Publication No. 4-348517 further in view of the Houston reference. This rejection is respectfully traversed for at least the following reasons.

Claim 1

A purpose of the present invention as described on page 2, lines 15-17 of the present application is to reduce cross-sectional area of a fuse. As described in the last paragraph on page 1 of the present application, a fuse is blown by Joule heat from a current that flows through the fuse itself. The Joule heat rises as the cross-sectional area of the fuse becomes small. The present invention uses a dielectric sidewall structure in order to narrow a through hole of the fuse, so as to reduce cross-sectional area of the fuse and to thus aid in fuse design and reduce overall size of semiconductor devices.

The semiconductor device of claim 1 includes in combination a dielectric sidewall structure "formed on the side face of the through hole so that the dielectric sidewall structure gradually narrows the through hole"; and a fuse "formed of a conductive material that buries the narrowed through hole, said

fuse having a lower end connected to the first conductive layer and an upper end connected to the second conductive layer". Appellant respectfully submits that the semiconductor device of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

The Examiner has primarily relied upon Fig. 14 of the Weber et al. reference. The Examiner has however acknowledged that the sidewalls within fuse hole 102 as illustrated in Fig. 14 of the Weber et al. reference are not gradually narrowed and are not a dielectric sidewall structure. In order to overcome these acknowledged deficiencies of the Weber et al. reference, the Examiner has relied upon Japanese Patent Publication No. 4-348517 as disclosing a contact hole with a polycrystalline semiconductor sidewall that narrows the hole towards the base of the hole, as illustrated in Figs. 7 and 12. The Examiner has further relied upon the Houston reference as disclosing in Fig. 1b a sub-lithographic opening for a back contact or back gate, wherein the sidewall spacers 108 that gradually narrow the hole/opening 106 are an oxide dielectric.

The Examiner has alleged on page 3, lines 5-8 of the Final Office Action dated August 11, 2005, that it would have been obvious "to include the required hole narrowing and the required insulating/dielectric sidewall spacers in Weber et al. [a] as taught by JP 04348517 and Houston respectively, in order to have a semiconductor device with increased performance". Appellant respectfully disagrees for the following reasons.

As described beginning in column 6, line 14 of the Weber et al. reference with respect to Fig. 14, fuse hole 102 includes a CVD aluminum wetting layer 114 on a liner material layer 104 such as stacked implanted titanium and/or a CVD TiN. Accordingly, fuse hole 102 in Fig. 14 of the Weber et al. reference includes **first and second conductive layers** lining the inner walls thereof, and consequently the cross-sectional area of the fuse is thus the same as the cross-sectional area of the contact hole itself. In other words, the Weber et al. reference does not disclose or suggest the concept of narrowing cross-sectional area of a fuse by lining the sidewalls of a fuse hole with a dielectric material.

As emphasized on pages 8-9 of the Amendment filed May 26, 2005 in connection with the present application, Japanese Patent Publication No. 4-348517 discloses **a conductive sidewall** in a **contact hole**. However, Japanese Patent Publication No. 4-348517 as relied upon by the Examiner does not specifically describe a fuse or a fuse hole. Also, the sidewall within the contact hole in Japanese Patent Publication No. 4-348517 is conductive. Japanese Patent Publication No. 4-348517 therefore does not disclose or suggest the concept of reducing a cross-sectional area of a fuse by lining the sidewalls of a fuse hole with a dielectric material.

The Houston reference as relied upon by the Examiner discloses a low resistance buried **back contact** for SOI devices as illustrated in Fig. 1b, wherein oxide sidewalls 108 are deposited within trench 106. However, as acknowledged by the Examiner and as noted above, the Houston reference is

concerned with buried back contacts for SOI devices, not with fuses. The Houston reference does not disclose a fuse, or a fuse hole. The Houston reference as relied upon by the Examiner thus does not disclose or suggest the concept of reducing a cross-sectional area of a fuse by lining the sidewalls of a fuse hole with a dielectric material. Accordingly, the prior art as relied upon by the Examiner taken singularly or together does not disclose or suggest the features of claim 1.

Appellant further respectfully submits that the Examiner has not established sufficient motivation to modify the fuse structure of the Weber et al. reference in view of the secondarily relied upon references. One of ordinary skill, looking to improve a fuse structure, would have no motivation to consider Japanese Patent Publication No. 4-348517 which discloses narrowing contact holes using polycrystalline semiconductor sidewalls, or the Houston reference which discloses forming sidewalls within low resistance buried back contacts for SOI devices. Since the secondarily relied upon references are not directed to fuses, it is not understood how these secondary references could motivate one of ordinary skill to modify conductive liner layers 114 and 104 of the vertical fuse illustrated in Fig. 14 of the Weber et al. reference. That is, it is unclear how teachings specifically directed to a contact hole and/or low resistance back contacts for a back gate could provide any motivation to modify a fuse, or more particularly to modify conductive liner layers of a vertical fuse. Accordingly, one of ordinary skill would not consider these

secondary references in an effort to modify the fuse device of the Weber et al. reference to have "increased performance", as suggested by the Examiner.

Moreover, the Examiner has failed to explain how the teaching of polycrystalline semiconductor sidewalls that narrow a contact hole as in Japanese Patent Publication No. 4-348517, or the teaching of an oxide sidewall in a low resistance buried back contact as in the Houston reference, would provide for "increased performance" of the vertical fuse in Fig. 14 of the Weber et al. reference. In absence of such specifically established motivation as provided in the relied upon prior art, this rejection would appear to be based merely upon impermissible hindsight and thus clearly improper.

With further regard to this rejection, the Examiner has failed to clearly explain how the vertical fuse structure would be modified in view of the secondarily relied upon prior art to meet the features of claim 1. The Examiner has thus presumably suggested replacing aluminum wetting layer 114 and titanium (or TiN) layer 104 in Fig. 14 of the Weber et al. reference with both a polycrystalline semiconductor sidewall as in Japanese Patent Publication No. 4-348517 **and** an oxide sidewall as in the Houston reference. Even if proper motivation existed for combining the prior art as suggested by the Examiner (which motivation Appellant does not admit exists), it is unclear how the teachings as combined would meet the features of claim 1.

On page 2 of the Advisory Action dated November 4, 2005, the Examiner has merely repeated the gist of the prior art rejection. That is, the Examiner has reiterated the manner in which the relied upon prior art has

been interpreted to correspond to the features of the claims. The Examiner has however failed to establish the necessary motivation for modifying the primarily relied upon Weber et al. reference in view of the secondarily relied upon prior art.

Appellant therefore respectfully submits that the semiconductor device of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 1-3 and 5-7 is improper for at least these reasons.

Claim 3

Claim 3 further features that the dielectric sidewall structure of the semiconductor device of claim 1 "includes a first layer formed on the side face of the through hole and a second layer formed on the first layer". However, as noted above, it would appear that the Examiner has suggested replacing aluminum wetting layer 114 and titanium (or TiN) layer 104 in Fig. 14 of the Weber et al. reference with both a polycrystalline semiconductor sidewall as in Japanese Patent Publication No. 4-348517 **and** an oxide sidewall as in the Houston reference. The prior art as presumably combined by the Examiner thus would not include a dielectric sidewall structure including a first layer on a second layer, because at least one of the layers of the sidewall of the combined prior art as relied upon by the Examiner would necessarily be a polycrystalline semiconductor.

The prior art as relied upon by the Examiner taken singularly or together therefore fails to meet or make obvious the features of claim 3. Appellant

therefore respectfully submits that the semiconductor device of claim 3 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection is improper for at least these additional reasons.

Claim 9

The semiconductor device of claim 9 includes in combination a dielectric sidewall structure "formed on a side surface of the through hole so that the dielectric sidewall structure gradually narrows the through hole"; and a conductive material "filled in the narrowed through hole".

Appellant respectfully submits that the prior art as relied upon by the Examiner taken singularly or together does not disclose or suggest the concept of gradually narrowing cross-sectional area of a fuse by lining the sidewalls of a fuse hole with a dielectric material. Japanese Patent Publication No. 4-348517 as secondarily relied on discloses a conductive sidewall in a contact hole. The Houston reference as secondarily relied on discloses a low resistance buried back contact for SOI devices, wherein oxide sidewalls are deposited within a trench. Appellant respectfully submits that the Examiner has not established sufficient motivation to modify the fuse structure of the Weber et al. reference in view of the secondarily relied upon references. Moreover, the Examiner has failed to explain how the teaching of polycrystalline semiconductor sidewalls that narrow a contact hole as in Japanese Patent Publication No. 4-348517, or the teaching of an oxide sidewall in a low resistance buried back contact as in the Houston reference,

would provide for "increased performance" of the vertical fuse in Fig. 14 of the Weber reference. Appellant therefore respectfully submits that the semiconductor device of claim 9 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 9-11 and 13-15 is improper for at least these reasons.

Claim 11

Claim 11, as dependent upon claim 9, features that the dielectric sidewall structure "includes a first sidewall film formed on the side surface of the through hole and a second sidewall film formed on the first sidewall film". However, as noted above, the Examiner has presumably suggested modifying the vertical fuse in Fig. 14 of the Weber et al. reference so as to replace aluminum wetting layer 114 and titanium (or TiN) layer 104 with both a polycrystalline semiconductor sidewall as in Japanese Patent Publication No. 4-348517 **and** an oxide sidewall as in the Houston reference. The prior art as presumably combined by the Examiner thus would not include a dielectric sidewall structure including a first layer on a second layer, because at least one of the two layers of the sidewall of the combined prior art would necessarily be a polycrystalline semiconductor. The combined prior art as relied upon by the Examiner would thus fail to meet or make obvious the features of claim 11. Appellant therefore respectfully submits that claim 11 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 11 is improper for at least these additional reasons.

Claim 15

Claim 15, as dependent upon claim 11, features that "the first sidewall film is formed of silicon nitride and the second sidewall film is formed of silicon oxide". Appellant respectfully notes that these features are somewhat similar to the features as set forth in dependent claim 8.

As acknowledged by the Examiner in the Allowable Subject Matter section at the top of page 2 of the Final Office Action dated August 11, 2004, claim 8 has been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Appellant thus respectfully submits that claim 15 should be considered as including allowable subject matter for at least somewhat similar reasons as claim 8. Appellant therefore respectfully submits that claim 15 distinguishes over and would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together for at least these additional reasons.

Claim 16

Claim 16 includes in combination a dielectric sidewall structure "formed in the through hole so that the through hole is gradually narrowed by the dielectric sidewall structure to expose the first conductive film"; and a fuse structure "formed by a conductive material filled in the narrowed through hole". Appellant respectfully submits that the prior art as relied upon by the Examiner taken singularly or together does not disclose or suggest the concept of narrowing cross-sectional area of a fuse by lining the sidewalls of a fuse hole

with a dielectric material. Japanese Patent Publication No. 4-348517 as secondarily relied on discloses a conductive sidewall in a contact hole. The Houston reference as relied on discloses a low resistance buried back contact for SOI devices, wherein oxide sidewalls are deposited within a trench. Applicant respectfully submits that the Examiner has not established sufficient motivation to modify the fuse structure of the Weber et al. reference in view of the secondarily relied upon references. Moreover, the Examiner has failed to explain how the teaching of polycrystalline semiconductor sidewalls that narrow a contact hole as in Japanese Patent Publication No. 4-348517, or the teaching of an oxide sidewall in a low resistance buried back contact as in the Houston reference, would provide for "increased performance" of the vertical fuse in Fig. 14 of the Weber et al. reference. Appellant therefore respectfully submits that the semiconductor device of claim 16 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 16-20 is improper for at least these reasons.

Claim 18

Claim 18, as dependent upon claim 16, features that the dielectric sidewall structure "includes a first sidewall film formed on a side surface of the through hole and a second sidewall film formed on the first sidewall film". However, as noted above, the Examiner has presumably suggested modifying the vertical fuse in Fig. 14 of the Weber et al. reference so as to replace aluminum wetting layer 114 and titanium (or TiN) layer 104 with both a

polycrystalline semiconductor sidewall as in Japanese Patent Publication No. 4-348517 **and** an oxide sidewall as in the Houston reference. The prior art as presumably combined would not include a dielectric sidewall structure including a first layer on a second layer, because at least one of the two layers of the sidewall of the combined prior art would necessarily be a polycrystalline semiconductor. The combined prior art as relied upon by the Examiner would thus fail to meet or make obvious the features of claim 18. Appellant therefore respectfully submits that claim 18 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 18 is improper for at least these additional reasons.

VIII. CONCLUSION

Appellant respectfully submits that claims 1-3, 5-7, 9-11 and 13-20 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together. Appellant therefore respectfully requests that the final rejection of claims 1-3, 5-7, 9-11 and 13-20 be withdrawn, and that these corresponding claims be passed to issue in the present application.

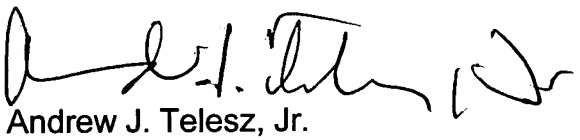
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. 41.20, particularly extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

11951 Freedom Drive, Suite 1260
Reston, VA 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740

Claims Appendix

1) A semiconductor device comprising:

a substrate;

a first insulator layer formed on the substrate;

a first conductive layer formed on the first insulator layer;

a second insulator layer formed on the first conductive layer, the second insulator layer including a through hole having a substantially vertical side face;

a second conductive layer formed on the second insulator layer;

a dielectric sidewall structure formed on the side face of the through hole so that the dielectric sidewall structure gradually narrows the through hole; and

a fuse formed of a conductive material that buries the narrowed through hole, said fuse having a lower end connected to the first conductive layer and an upper end connected to the second conductive layer.

2) A semiconductor device according to claim 1, wherein the fuse and the second conductive layer are formed of a same material.

3) A semiconductor device according to claim 1, wherein the dielectric sidewall structure includes a first layer formed on the side face of the through hole and a second layer formed on the first layer.

4) A semiconductor device according to claim 1, wherein a thickness of the dielectric sidewall structure is smallest at the substrate and becomes gradually larger away from the substrate.

5) A semiconductor device according to claim 1, wherein the first and second conductive layers are interconnections.

6) A semiconductor device according to claim 1, wherein the first and second conductive layers are made of aluminum.

7) A semiconductor device according to claim 1, wherein the first and second insulator layers are made of silicon oxide.

8) A semiconductor device according to claim 3, wherein the first layer is formed of silicon nitride and the second layer is formed of silicon oxide.

9) A semiconductor device comprising:

a semiconductor substrate;

a first dielectric film formed on the semiconductor substrate;

a first conductive film formed on the first dielectric film;

a second dielectric film formed on the first conductive film, the second dielectric film including a through hole that exposes the first conductive film;

a dielectric sidewall structure formed on a side surface of the through hole so that the dielectric sidewall structure gradually narrows the through hole;

a conductive material filled in the narrowed through hole; and

a second conductive film on the second dielectric film and the conductive material, so that the conductive material electrically connects the first and second conductive films to each other.

10) A semiconductor device according to claim 9, wherein the conductive material and the second conductive film are formed of a same material.

11) A semiconductor device according to claim 9, wherein the dielectric sidewall structure includes a first sidewall film formed on the side surface of the through hole and a second sidewall film formed on the first sidewall film.

12) A semiconductor device according to claim 9, wherein a thickness of the dielectric sidewall structure is smallest at the semiconductor substrate and becomes gradually larger away from the semiconductor substrate.

13) A semiconductor device according to claim 9, wherein the first and second conductive films are made of aluminum.

14) A semiconductor device according to claim 9, wherein the first and second dielectric films are made of silicon oxide.

15) A semiconductor device according to claim 11, wherein the first sidewall film is formed of silicon nitride and the second sidewall film is formed of silicon oxide.

16) A semiconductor device comprising:

a semiconductor substrate;

a first conductive film formed on the semiconductor substrate;

a dielectric film formed on the first conductive film and the semiconductor substrate, the dielectric film having a through hole that exposes the first conductive film;

a dielectric sidewall structure formed in the through hole so that the through hole is gradually narrowed by the dielectric sidewall structure to expose the first conductive film;

a fuse structure formed by a conductive material filled in the narrowed through hole; and

a second conductive film on the dielectric film and the fuse structure, so that the fuse structure electrically connects the first and second conductive films to each other.

17) A semiconductor device according to claim 16, wherein the second conductive film is formed of the conductive material.

18) A semiconductor device according to claim 16, wherein the dielectric sidewall structure includes a first sidewall film formed on a side surface of the through hole and a second sidewall film formed on the first sidewall film.

19) A semiconductor device according to claim 16, wherein the first and second conductive films are made of aluminum.

20) A semiconductor device according to claim 16, wherein the dielectric film is made of silicon oxide.

Evidence Appendix

No evidence has been submitted under 37 C.F.R. 1.130, 1.131, or 1.132, or entered by the Examiner in connection with this pending Appeal.

Thus, there are **no** copies of evidence included in this Appendix.

Related Proceeding Appendix

There are no appeals or interferences that may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this pending Appeal. Thus, there are **no** copies of decisions included in this Appendix.